IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Songjie Xu
Appl. No.	:	09/754,406
Filed	:	January 2, 2001
For	:	METHODOLOGY AND APPLICATIONS OF TIMING DRIVEN LOGIC RESYNTHESIS FOR VLSI CIRCUITS
Examiner	:	Thomas H. Stevens
Group Art Unit	:	2123

CERTIFICATE OF MAILING

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on

May 1, 2006
(Date)

Raimond J. Salenieks, Reg. No. 37,924

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated November 2, 2005, Applicant submits the following remarks for consideration in connection with the above-identified patent application.

Summary of Interview begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

SUMMARY OF INTERVIEW

Exhibits and/or Demonstrations

None

Identification of Claims Discussed

Claims 1, 6, 9, 11, 21, and 25

Identification of Prior Art Discussed

Bennett et al., U.S. Patent No. 5,648,913

Proposed Amendments

None – the claims are unchanged

Principal Arguments and Other Matters

The Bennett reference does not disclose every element of each of Applicant's independent claims.

Results of Interview

It was discussed and agreed that Bennett does not disclose all the elements of each of the independent claims, such as, for example, those relating to certain orderings related to delay reduction, recursive reducing of delays, and iterative delay reduction. It was agreed by the Examiner that the Bennett reference was overcome and the claims appear to be allowable.